



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Kleint, et al.

Attorney Docket: 2002 P 14454 US

Filed: December 12, 2003

Examiner: TBD

Serial No.: 10/735,411

Art Unit: 2186

For: Method for Fabricating Semiconductor Memories with Charge Trapping Memory Cells

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

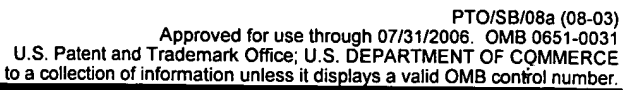
Respectfully submitted,

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April 7, 2004

Date

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

**Complete if Known**

Application Number	10/735,411
Filing Date	12/12/2003
First Named Inventor	Kleint, et al.
Art Unit	2186
Examiner Name	TBD
Attorney Docket Number	2002 P 14454 US

Sheet	1	of	1
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[illegible][illegible]Date  
Considered

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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